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Chambers

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[54] **VISUAL DISPLAY SYSTEM**

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[73] Assignee: **Raytheon Company**, Lexington, Mass.

[22] Filed: **May 7, 1973**

[21] Appl. No.: **358,212**

Related U.S. Application Data

[62] Division of Ser. No. 143,343, May 14, 1971.

[52] **U.S. Cl.** ..... **340/172.5**, 340/324 A

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** ..... 340/172.5, 324 A, 324 AD

[56] **References Cited**

UNITED STATES PATENTS

3,388,391	1/1968	Clark	340/324
3,418,518	12/1968	Reese, Jr.	340/324 AD
3,422,420	1/1969	Clark	340/324 AD
3,581,290	5/1971	Sugarman	340/172.5
3,597,757	8/1971	Vincent-Carrefour	340/324 A
3,611,348	10/1971	Rogers	340/324 A
3,685,039	8/1972	Flanagan	340/324 A
3,701,988	10/1972	Allaart	340/324 A

Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—J. D. Pannone; M. D. Bartlett; J. R. Inge

[57] **ABSTRACT**

An enhanced alphanumeric character display system in which a raster scan dot matrix is generated at a plurality of display locations with local computer control over local groups of displays is disclosed. Data from the generation of an individual dot matrix characters is locally stored in a recirculating register independently from a random access refresh memory thereby removing the recirculation function from the refresh memory. A technique for shifting selected dots in the character matrix to obtain improved characters is also disclosed.

10 Claims, 12 Drawing Figures

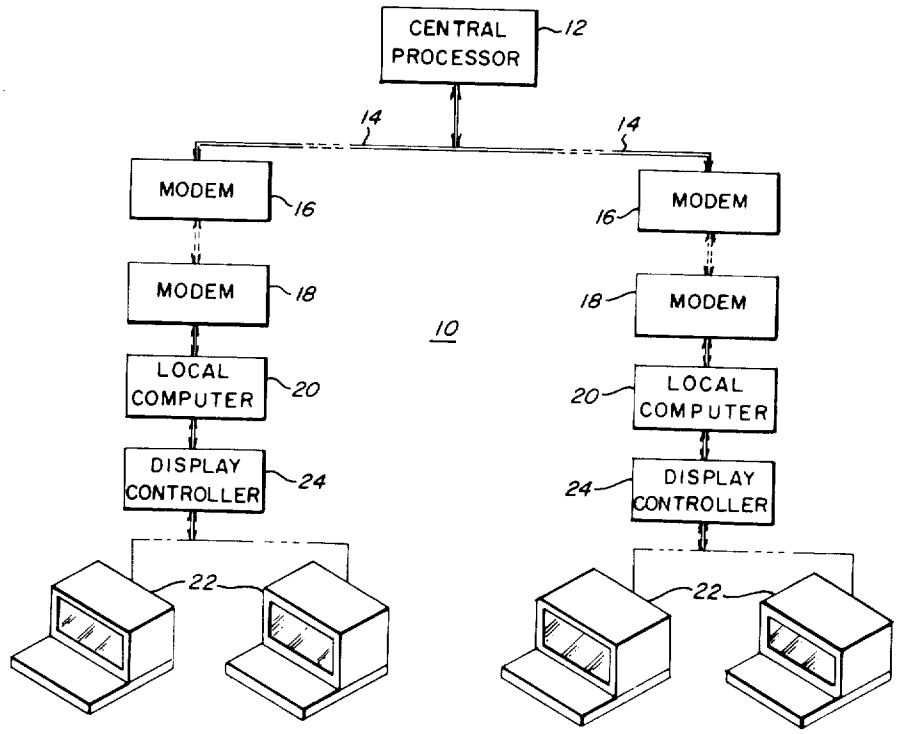
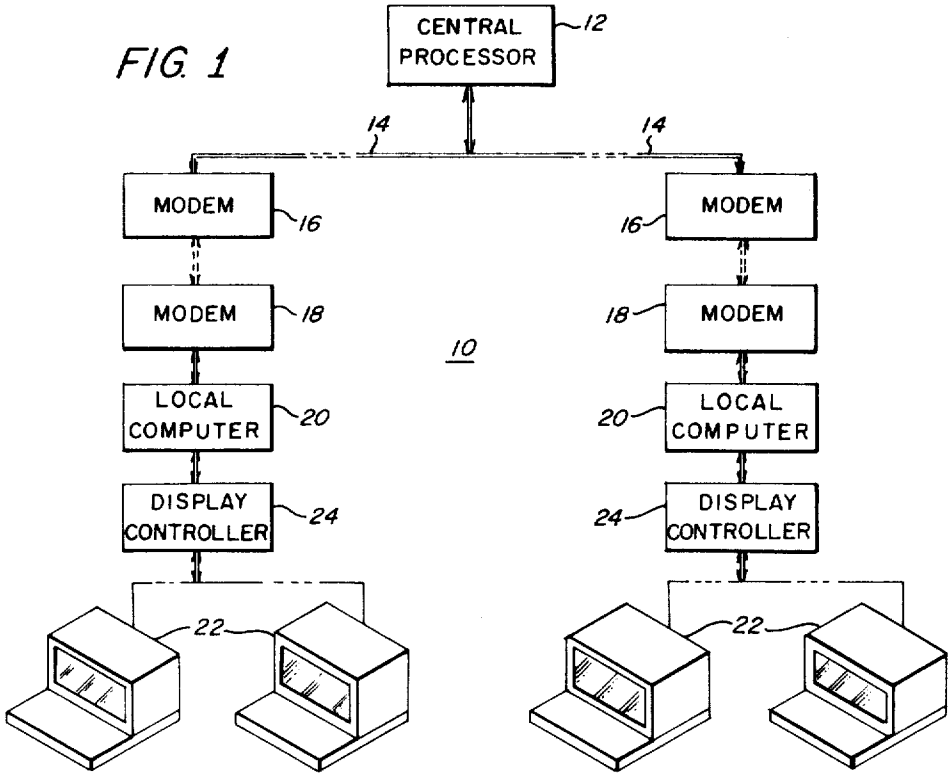


FIG. 1


CENTRAL PROCESSOR
12
14
14
MODEM
16
MODEM
16
MODEM
18
MODEM
18
10
LOCAL COMPUTER
20
LOCAL COMPUTER
20
DISPLAY CONTROLLER
24
DISPLAY CONTROLLER
24
22
22

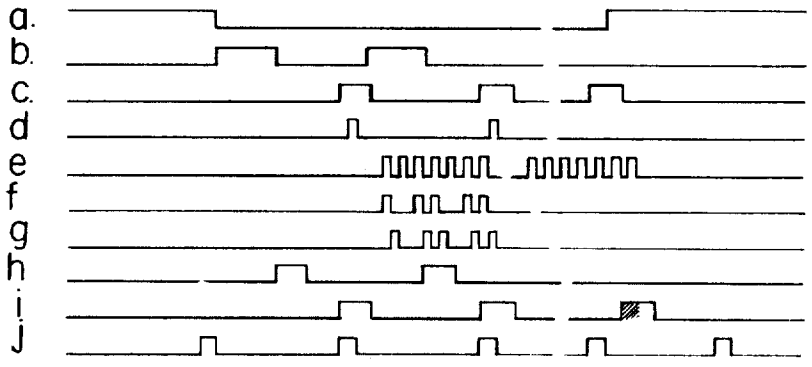

a.
b.
c.
d
e
f
g
h
i
j

FIG. 11

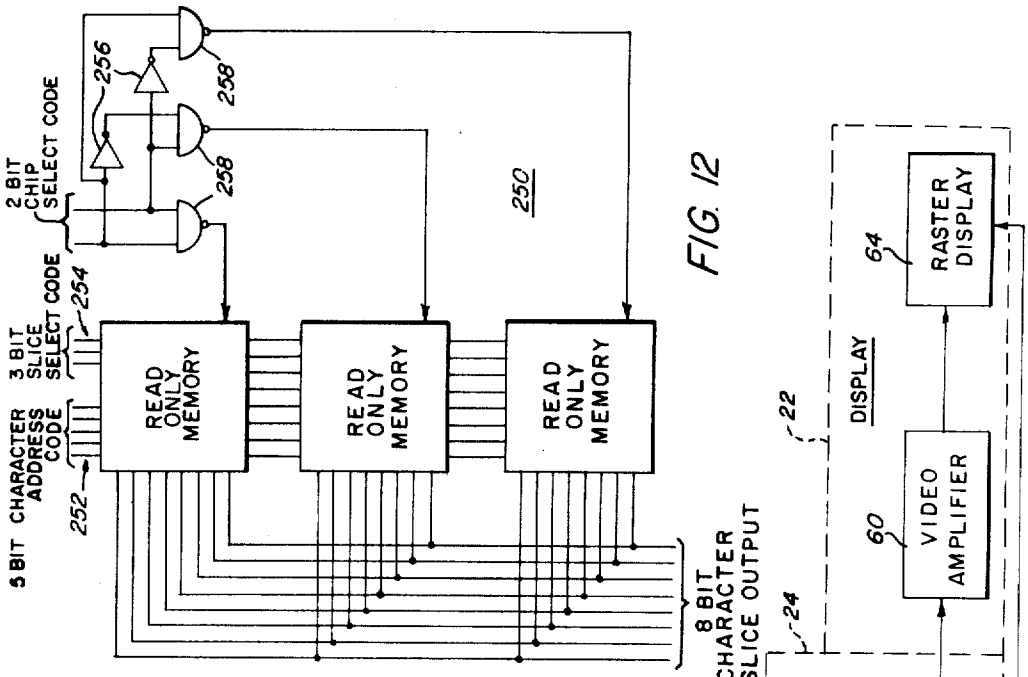

2 BIT CHIP SELECT CODE
256
258
258
3 BIT SLICE SELECT CODE
254
5 BIT CHARACTER ADDRESS CODE
252
READ ONLY MEMORY
READ ONLY MEMORY
READ ONLY MEMORY
250
8 BIT CHARACTER SLICE OUTPUT
24
22
DISPLAY
64
RASTER DISPLAY
60
VIDEO AMPLIFIER
58
DOT SHIFT CIRCUIT
56
READ ONLY MEMORY
55
ROW STORE
52
RANDOM ACCESS DISPLAY MEMORY
TO OTHER DISPLAYS
DISPLAY CONTROLLER
FROM LOCAL COMPUTER
54
LOCAL COMPUTER INTERFACE
62
SYSTEM TIMING
KEYBOARD
50

FIG. 12

FIG. 2

5X7 MATRIX

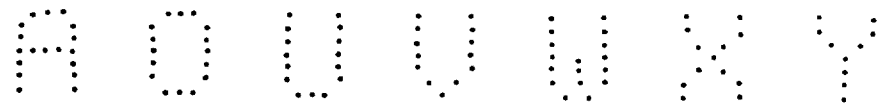


FIG. 3

7X9 MATRIX

FIG. 4

7 X 7 MATRIX

FIG. 5

ENHANCED 7 X 7 MATRIX

FIG 6

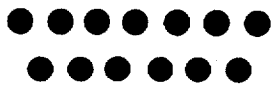


FIG. 7

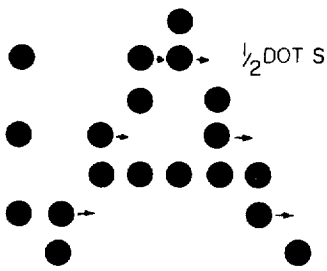


FIG. 8

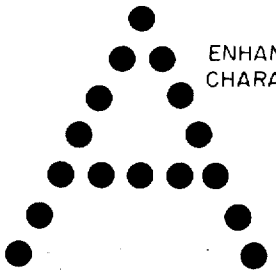
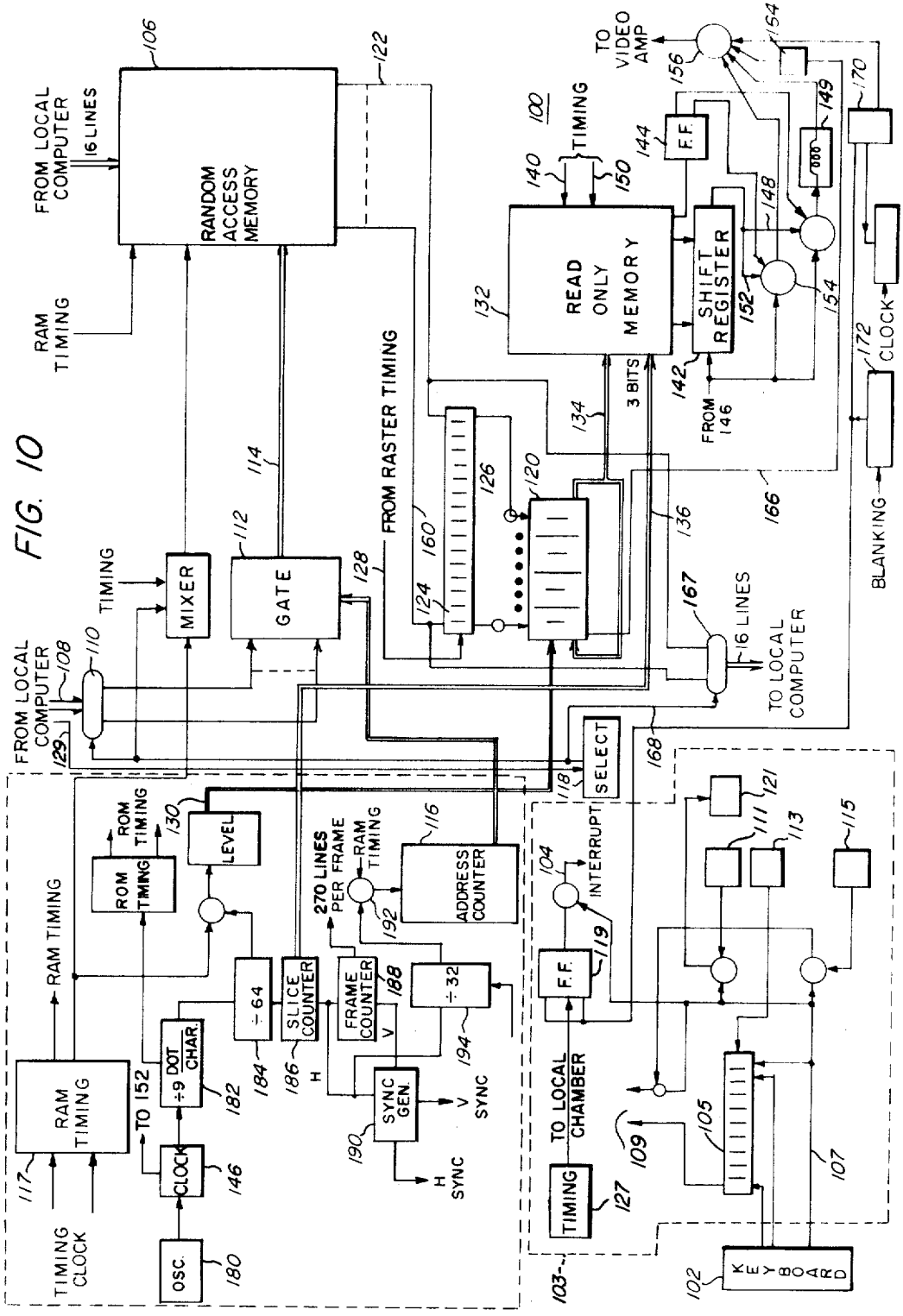


FIG. 9

FIG. 10


FROM LOCAL COMPUTER
16 LINES
RANDOM ACCESS MEMORY
RAM TIMING
TO VIDEO AMP
TIMING
READ ONLY MEMORY
SHIFT REGISTER
F.F.
3 BITS
FROM 146
CLOCK
BLANKING
FROM RASTER TIMING
MIXER
GATE
TIMING
16 LINES
TO LOCAL COMPUTER
SELECT
ROM TIMING
LEVEL
270 LINES PER FRAME
RAM TIMING
ADDRESS COUNTER
INTERRUPT
RAM TIMING
÷ 64
SLICE COUNTER
FRAME COUNTER
÷ 32
÷9 DOT CHAR.
SYNC GEN.
TO 152
TO LOCAL CHAMBER
TIMING
CLOCK
OSC.
TIMING CLOCK
KEYBOARD

VISUAL DISPLAY SYSTEM

This is a division of application Ser. No. 143,343 filed May 14, 1971.

BACKGROUND OF THE INVENTION

This invention relates to a dot matrix type visual display system in which alphanumeric characters are developed by a raster type scan on a viewing screen such as a cathode ray tube.

In many data display and communication systems, such as those used with digital computers, it has been found useful to display the processed information as alphanumeric characters on a cathode ray tube or other display means. The cost of such a display device is significantly reduced by the use of a conventional raster scan monitor with a cathode ray tube, which monitor could be a television set without the radio frequency and intermediate frequency sections. Typically, characters have been formed in the prior art from a dot matrix in which a cluster of dots form characters on the screen by unblanking the raster sweep of the electron beam at selected intervals which correspond to points on the matrix. Such systems do not produce characters with the resolution of stroke generators or monoscope systems, as the characters are not continuous lines, but rather a plurality of dots. Additionally, because of the matrix geometry, true letter shapes are not obtainable from a conventional dot matrix for many characters unless the matrix is expanded to include more closely spaced dots, with an accompanying increase in cost, circuit complexity and bandwidth requirements.

An additional problem in dot matrix visual display systems of the prior art, and of other cursive displays, including those of the target monoscope type, is the requirement that a portion of the local computer memory be dedicated to refreshing the display. Thus, interface circuitry, such as character entry and readout registers, delay lines and gating circuitry are required to couple data to the display from that portion of the local computer memory which forms a portion of the refresh memory.

SUMMARY OF THE INVENTION

The above problems and other problems of the prior art are overcome by the present invention, in which an enhanced dot matrix display is developed by a raster scan. In accordance with the present invention, the characters to be generated are stored in a read only memory which is accessed by character address codes that are recirculated in a recirculating shift register. This shift register contains sufficient data to generate one line of characters, and recirculation therein is independent from the local memory, which in the instant invention is a random access memory. Thus, the processor is free to perform functions other than refreshing the display with a consequent improvement in system efficiency, cost and circuit complexity.

In the present display, each character, for example, may comprise seven parallel lines containing seven dots per line for a seven by seven dot matrix. The top line of dots for all of the characters in the row is generated first, then the second, and so forth until the seventh line is generated, whereupon several lines are skipped, for example six, and the next row of characters is generated until a complete frame of lines is displayed. Selected dots in the character matrix are laterally displaced from their normal position in the matrix by delaying the dot generation signals by one-half of the interdot space in order that enhanced characters are produced. The effect is the same as if the number of dots in the matrix were increased, but without the additional circuit complexity and bandwidth requisite by such an approach.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages of the invention will become apparent from the following specification taken in connection with the accompanying drawings wherein like reference characters identify parts of like function throughout the different views thereof and wherein several of the views double lines indicate data flow.

FIG. **1** is an overall system block diagram of a visual display system embodying the present invention;

FIG. **2** is a block diagram of an individual display embodying the present invention;

FIGS. **3** through **5** are characters formed by dot matrices of the prior art;

FIG. **6** is an enhanced dot matrix formed in accordance with the teaching of the present invention;

FIG. **7** illustrates the dot shift in accordance with the present invention;

FIGS. **8** and **9** illustrate the formation of a single enhanced character in accordance with the teachings of the present invention;

FIG. **10** is a detailed block diagram of a dot matrix visual display system in accordance with the present invention;

FIG. **11** is a series of waveforms of various signal generated throughout the block diagram illustrated by FIG. **10**; and

FIG. **12** is a block diagram of the read only memory employed by the block diagram of FIG. **10**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. **1**, a data communications system embodying the present invention is shown generally at **10**. Digital information in binary form is stored at a central processing unit (CPU) **12**, which may be an IBM type **360** computer, which is coupled to the individual programmable displays via data lines **14**, which may be telephone lines. Input and output modems **16** and **18**, which may be a Western Electric type **201**, respectively transmit and receive data such as character codes between the central processor **12** and a small programmable local computer unit **20** which includes a computer, such as a Raytheon type **704** computer.

Each local unit **20** controls a cluster of displays **22** by coupling digital information to a display controller **24**. In the present embodiment, each controller **24** controls eight displays; however, the system may be expanded to accommodate any number of displays **22**. Additionally, other modems, not shown, couple data from the CPU to other locally programmable units similar to unit **20**, such that the system is expandable to many clusters of displays at a plurality of spaced locations.

While various display configurations are possible, such as a single output channel with one refresh memory, one character generator and a raster-scan monitor interface that is capable of driving two one-thousand character monitors or four five-hundred character monitors; the preferred embodiment is a fully expandable system with up to eight channels, each channel

being capable of driving either one 2,000-character display, two 1,000-character displays, or four 500-character displays.

When more than one television monitor display **22** is connected to an output channel of each local computer unit **20** through a display controller **24**, conventional local monitor interface circuitry provides the keyboard multiplexing, split timing and blanking signals required to time-share the memory and character generator between the displays **22**.

Referring now to FIG. **2**, a block diagram of a display controller **24** and a display **22** with a keyboard **57** is illustrated generally at **50**. A random access display memory **52** at any desired location such as a local computer **20** or as shown in display controller **24** stores character address codes sufficient to produce a frame of data on a raster screen. The capacity of random access memory **52** is such that it contains data frames for a plurality of displays and only a portion of the memory is actually used for any one display. In accordance with the present invention, the frame storage portion of the random access memory allocated to each display does not perform any of the refresh function, i.e., character address recirculation, as this is accomplished on a line by line basis in a recirculating shift register or registers thereby freeing the random access memory **52** for other processing tasks.

Data changes made by keyboard entries are coupled through the local computer interface **54** to the random access memory **52** for character changes. Data is coupled a row of character address codes at a time from random access memory **52** to a line store **55** in which data sufficient to generate one row of the raster display is recirculated and nondestructively coupled to the address inputs of a read only memory **56**. The data is recirculated once for each of the scan lines in a row of characters. It is thus apparent that any portion of memory **52** is unnecessary for data recirculation. Hence, more flexibility is effected in both memory storage space and system operation as independent row storage is achieved without reliance on the recirculating random access memory **52** or on any external delay line, although, of course, such a line may be used if desired. Data in dot bit form is generated by the read only memory, with seven of the eight generated dot bits corresponding to one character slice. The number of character slices required for the generation of particular characters as will be described in more detail with reference to FIG. **10** is coupled to dot shift circuit **58** where selected dots in selected character slices are shifted by one-half space or any desired amount in order to form enhanced characters as described with respect to FIG. **10** and other unshifted data along with the shifted data is applied in pulse form to video amplifier **60** at the raster display which pulses are used to unblank the raster scan to generate the required dot pattern. Conventional system timing **62** synchronizes the random access display memory with read only memory and develops both horizontal and vertical synchronization for application to the raster display **64**.

Referring now to FIGS. **3** through **9**, various dot matrices are illustrated and compared with the enhanced dot matrix achieved by the present invention. FIGS. **3** through **5** illustrate the best that can be done for dot positioning on the given matrix sizes without using the dot shift technique of the present invention. FIG. **6** illustrates the improvements that are possible with the 7 by 7 matrix when dot shift technique is used. The minimum dot matrix size for recognizable upper case alphanumeric characters illustrated by FIG. **3** is generally considered to be one comprising **5** by **7** dots arranged in a matrix of parallel, horizontal and vertical columns of dots. While increasing the number of dots in the matrix improves resolution, additional storage and video bandwidth are required with the consequent decrease in number of displayed character rows. For monitor type raster displays, a matrix allowing good character quality and the possibility of adding lower case characters is desirable. These requirements can be satisfied in a 7 by 9 dot matrix such as that illustrated by FIG. **4** in which the upper case characters A, O, U, V, W, X and Y are illustrated. When the matrix of FIG. **4** is used in a conventional unshifted type dot matrix of the prior art to present both upper and lower case characters the upper case characters, assuming that they are confined to the upper 7 by 7 dot portion of the matrix leave the lower two rows of dot for the tails of the lower case character. The effect on character shape and definition of such a system is illustrated by FIG. **5** in which the distortion and the letter shape is clearly apparent.

Referring now to FIG. **6**, the characters generated in accordance with the present invention are illustrated. By way of example the letter A is clearly enhanced by the shifting of several selected dots in the matrix resulting in more legible character shapes which may be produced without increasing video bandwidth or decreasing the number of displayed character lines. Only the addition of one column of bits, per character is required to be stored in the character generator read only memory along with the 7 by 7 stored dot matrix to achieve the enhancement shown in FIG. **6**. Each of the extra bits located in the far left column of dots in FIG. **8**, is used to control the shifting of all dots in a horizontal line with it for the particular character with which the bit is stored. This enables either the original 7 normal dot positions shown in FIG. **7** to be available, or the six positions spaced equally between them as illustrated. The letter A shown in FIGS. **8** and **9** is illustrative of the improvement resulting when character dots are shifted one-half space in accordance with a delay coding which for a shift could be a logical one and for no shift a logical zero.

As described with reference to FIG. **10**, the shift may be generated upon detection of logical one in the control bit position, for example, a complementary clock phase may be used to gate the video or a delay of one-half bit time introduced through a video delay line as illustrated. Thus, it is to be understood that while the video delay line technique is described either a complementary clock or other means for delaying selected dots in particular character portions or slices may be used in accordance with the present invention.

Referring now to FIG. **10**, a block diagram of a dot matrix character generation system in accordance with the present invention is shown generally at **100**. A keyboard **102** containing the usual complement of character and function keys is present at each display **22** to enable an operator to have access to the local computer - for changing the information displayed on the display screen by the activation of selected keys. When a key on the keyboard **102** is depressed an interrupt signal is coupled to the local computer via line **104** to enable the computer to receive data or instruction de-

pending on whether a character key or a function key has been depressed.

The keyboard interface gating **103** is of well known design, with character data from a standard keyboard matrix being coupled in an eight bit code to keyboard gating **105** along with a strobe pulse on line **107** to gate keyboard data from gating **105** to the local computer via lines **109** and into memory **106.** Additional keyboard interface gates **111, 113, 115** and **121** allow internal timing pulses to clock the keyboard status to enable the transfer of data out of gating **105** in accordance with the strobe timing. The actual data clocking is provided by timing **127** which times a flip-flop **119** to gate the generated interrupt signal to the local computer to allow data to be strobed in.

Keyboard data is stored in a refresh memory such as random access display memory **106,** which memory is capable of storing keyboard data from a plurality of displays, thus for eight displays storing 2,000 characters each, 8K 16 bits of memory is required. In the illustrated embodiment, memory **106** is shown as storing data for one display, however, it may be easily expanded to accommodate any number of displays. Typically six or seven bits of data per character are required with an eighth bit for a movable cursor, with 7 bits resulting in up to **128** different character codes. In the illustrated embodiment, a 7 bit character code is employed with the eighth bit reserved for a cursor. A complete frame of data of, for example **24** rows of 80 characters per row with sixteen character spaces for horizontal retrace being **64** characters per row may be stored and recirculated through memory **106** which, in the illustrated embodiment, is capable of storing **1024** 16 bit words with two **8**-bit characters comprising each 16 bit word.

In order to access the memory **106** from the local computer, **10** address lines illustratively shown at **108** from the local computer are coupled via switch **110** through a gate **112** into the address lines **114** of the random access memory **106** which comprise **10** lines capable of addressing **1024** word locations in the memory. Alternatively, the memory **106** may be addressed from an address counter **116** to be described via gate **112.** Memory select logic **118** is activated by a decode signal on line **129** from the local computer when data is required to be written or read from the display memory and activation of memory select **118** serves to inhibit data from address counter **116** and switches gate **112** to allow address data from the local computer via switch **110** to be coupled to the memory **106.** When data is present on the display screen, address counter **116** sequentially addresses each word location in the memory as controlled by the RAM timing **117** to be described and the display timing which RAM timing is typically approximately **1** microsecond per character.

A recirculating memory, row store **120** is loaded a row at a time which in the present embodiment comprises **64** characters and **16** retrace intervals from the RAM via **16** data lines illustratively shown as **122.** Each line inputs a data bit at the RAM timing rate of **1** bit per microsecond to the line store **120** which comprises eight 80-bit shift registers operated in parallel. of course, other length shift registers may be employed depending only upon the data present in line store **120,** which data is coupled first to a byte switch **124** which divides the **16**-bit input into two **8**-bit character bytes and alternately parallel transfers the data contained by bits **1** through **8** and **9** through **16** via lines **126** to the line store **120.** The timing for the alternate word transfer is provided by the raster timing via line **128** and these data pulses occur during entry of the next line of data from the random access memory **106** into the row store.

In the preferred embodiment row store **120** employs dynamic shift registers, arranged such that any stoppage of clock pulses will not be of sufficient duration to result in loss of data. Normally, data is recirculated in registers **120** a number of times equivalent to the number of line scans of the raster necessary to write a character, typically this is **7** to **9** times, although in the present embodiment recirculation occurs **9** times. Clock pulses from the raster timing are inputted to the row store **120** via line **130** to clock data out of row store **120** and into the character generator read only memory **132** via 7 lines illustratively shown at **134** at the clock rate. The data is also of course recirculated in row store **120** during the parallel transfer from register **120** to read only memory **132.**

Read only memory **132** converts the 7-bit character code into video pulses which represent the various character portions or slices as illustrated by FIG. **8.** Seven rows of dots or character slices are required for the generation of each displayed character. Read only memory **132** may, for example, comprise **3** Intel MOS LSI ROM memory type **1301** with self-contained gating. The read only memory timing is received at ROM **132** from the timing generator on line **140.** The read only memory may be comprised of several chips of integrated circuitry as described with respect to FIG. **11,** with each chip section of read only memory **132** accepting **8** input address lines which can produce **32** characters for a **96** character total when the memory sections are employed. For each of the **256** locations in each chip, **8** output data bits are available with 7 bits generating one line of data per character and with the eighth bit used for shifting the character code. Lines **136,** the character slice address lines, input a 3 bit address code from the read only memory timing as previously described.

This three bit address code is coupled to read only memory **132** as additional coding bits along with the five bit character code on line **134** to comprise a standard eight bit data code. While the internal gating in memory **132** is standard, the unitary eight bit code in actuality derives from separate sources, with the three bit slice counter portion on line **136** being cyclical and the five bit portion on line **134** being random. Thus, character addressing and slice selection and incrementing is simplified to a single decoding operation by read only memory **132.**

The address lines **136** are inputted to the read only memory one bit prior to character display upon receipt of an appropriate timing signal via line **150** from the ROM timing. Character codes for **32** different characters are inputted to the memory **132** via lines **134** as previously described. Output data from the read only memory **132** is parallel transferred to an 8-bit shift register **142** with 7 dot bits going into register **142** and the eighth dot bit located in the seventh data bit location, with the shift bit being coupled to flip-flop **144** with the shift occurring during intercharacter time. A video clock **146** shifts the data serially out of register **142** to one of two paths, one of which path **148** is delayed by delay line **149** for one-half dot bit time which is typi-

cally 40 nanoseconds with the character dots being spaced about 40 nanoseconds apart. The alternative path 152 couples output data from register 142 to gate 154 at which point the data is gated to the video output gate 156 which is an OR gate for mixing the blanking signals. Depending upon the state of the eighth shift bit for each character portion or slice, data is either delayed or undelayed by coding the shift bit either a logical one or a logical zero, and a one-half dot shift is effected such that selected dots in selected slices of a character are delayed with the effect of producing character enhancement as illustrated by the exemplary letter A in FIGS. 8 and 9 in which dots in the second, fourth and sixth character slices are effectively shifted to produce more realistic characters when the shift bits are at a logical one.

A single cursor bit is coupled to the random access memory 106 in either the zero or eighth data bit position location which cursor bit is used for the generation of a movable cursor on the display screen. The cursor bit is coupled to byte switch 124 via line 160 in the most significant bit position, and is then coupled to the line store 120 via gate 162 into the most significant bit position in one of the eight parallel shift registers of line store 120 in accordance with the address received from memory 106. Whenever a logical one is detected by cursor generator 164 which generator receives the cursor bit, either a zero when no cursor is present or a logical one, via line 166 from the line store, a cursor is generated and coupled through gate 156 to the video amplifier of the raster scan for display.

A switch 167 routes data from the random access memory back to the local computer accumulator when it is required that data be put back into the local computer such as when a keyboard function is selected. Switch 167 is actuated by a signal from the memory select 118 via line 168 when the appropriate function key is selected. Blanking signals are gated through gate 170 via the input buffer 172. The required dot matrix is generated from a video which is normally blank except when data is written in accordance with conventional blanking techniques.

The raster scan timing for synchronization of internal and external clocking provided by the local computer, the keyboard interface, and the raster monitor, is provided by the raster scan timing which originates in a crystal oscillator 180 of approximately 24 megahertz which is divided down to 12 megahertz in the vertical clock 146 and is then further divided by nine in divide by nine counter 182 to synchronize the character slices, each of which slices comprises nine dots with seven actual dots and two intercharacter spaces. After division by counter 182 the clock signal is again divided by 64 in an additional counter 184 to obtain line timing of 64 characters per line before coupling to the slice counter 186 which counts eight lines to give three bits out for generating a 3-bit code for selection of one of eight possible slices per character. Frame counter 188 counts the number of lines per frame, typically 270 lines and is used to synchronize the video monitor with the RAM timing.

Horizontal and vertical synchronization is generated by synchronization generator 190 which synchronizes the vertical and horizonal pulses on the cathode ray tube and determines when the horizontal and vertical sweeps start. Of course, vertical synchronization is determined by the frame counter output and horizontal synchronization by the output of slice counter 186. For every thirty two transfers from random access memory 106 to byte switch 124 60 characters are transferred. This is timed by address counter 116 via gate 192 which couples the RAM timing to the address counter. The address counter is incremented 32 times by a divide by thirty two counter 194 with coupling through gate 192 to address counter 116 such that character addresses are generated between character rows.

Referring now to FIG. 11, certain of the more important waveforms present in the block diagram illustrated by FIG. 10 are shown.

Waveform 11(a) is the horizontal retrace pulse train, which is approximately 12.1 microseconds. The read only memory strobing is illustrated by waveform (b), which clocks data from line store 120 to memory 132, and data is read out of the read only memory by waveform (c) and strobed into register 152 by waveform (d). Shifting out of register 152 to the dot shift circuitry occurs in accordance with timing providing by waveform (e). Data flowing along path 152, the unshifted path, is illustrated by waveform (f) while shifted data with a one-half bit shift through delay line 149 is illustrated by waveform (g). Waveform (h) clocks data from the output of the line store for recirculating when data is read out to the memory 132, with shifting being accomplished in accordance with waveform (i). Waveform (j) illustrates the relationship between the character generation time and horizontal retrace.

Referring now to FIG. 12, read only memory 132 is illustrated generally at 250. A 5-bit character address code is inputted to memory 132 via data lines 252 from line store 120, which code defines one of 32 possible different characters per memory chip, for a total of ninety-six different possible characters as there are three chips. Of course, more or less read only memory may be utilized, depending only upon how many different characters are required. A three bit timing code on lines 254 from slice counter 186 is decoded by the memory 254 to select a particular row of characters. In the present embodiment, there are sixteen rows of displayed characters with nine lines per row from which characters may be formed with six lines between row for interrow spacing, and two character row for vertical retrace for a total of two hundred seventy slices, or horizontal raster scans per frame of data displayed. Each chip contains 32 eight bit locations in which character information is stored. As this data is clocked out a character slice at a time into register 142, the top slice of all of the characters in a row, or one ninth of the individual characters is displayed. These slices are incremented by the divide by 15 slice counter 186 until all of the characters in one row are displayed, and the fifteenth line clocks counter 186 to change the code on line 254 cyclically in order that character writing is incremented to the next row, and so on until the end of the frame, at which time the frame counter increments the row select code back to the first row for character refresh. A two bit chip select code is coupled to memory 132 from the line store 120 along with the character address code in order that the correct 32 character memory section is addressed. This code is coupled to the three memory sections in a conventional manner through standard gating such as that provided by inverters 256 and OR gates 258.

While particular embodiments of the invention have been shown and described, various modifications

thereof will be apparent to those skilled in the art and therefore it is not intended that the invention be limited to the disclosed embodiments or to details thereof and departures may be made therefrom within the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. Apparatus for generating a visual display of characters on a cathode ray tube in a raster;

said generated characters being formed from a dot matrix comprising means for generating a plurality of rows of characters each of which generated characters comprises a plurality of horizontal slices each of which slices comprises a plurality of dots such that each of said generated characters is comprised of a plurality of dots;

means for sweeping the electron beam of said cathode ray tube across the screen in a raster pattern such that said electron beam is normally blanked;

means for unblanking said electron beam in accordance with a predetermined instruction sequence such that a display of said characters is generated; and

means for displacing certain of said generated dots from their normal character positions such that an enhanced character display is produced, said displacing means operating independently of said electron beam sweeping means.

2. A visual display system in accordance with claim **1** wherein said character generating means comprises a read only memory.

3. A visual display system in accordance with claim **2** further comprising a recirculating memory for addressing said read only memory.

4. A visual display system in accordance with claim **3** wherein said read only memory has a plurality of output lines and further comprising means coupled to said output lines for sequentially coupling each of said output lines one at a time to said signal displacing means.

5. A visual display system in accordance with claim **4** wherein said coupling means comprises a shift register.

6. A visual display system in accordance with claim **1** wherein said signal displacing means comprises delay means.

7. A visual display system in accordance with claim **6** wherein said delay means comprises a flip-flop.

8. A visual display system in accordance with claim **6** wherein said delay means comprises a delay line.

9. A visual display system in accordance with claim **6** further comprising video amplifier means, the input of said video amplifier means being coupled to said delay means and the output of said video amplifier means being coupled to said cathode ray tube.

10. A visual display system in accordance with claim **1** wherein said signal displacing means comprises means for causing selected ones of said dots to be displayed shifted by substantially one-half the normal inter-dot spacing.

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